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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,934	11/26/2003	Michael Wayne Lane	YOR920030505US1 (163-21)	9639
24336	7590	06/16/2005	EXAMINER	
KEUSEY, TUTUNJIAN & BITETTO, P.C. 14 VANDERVENTER AVENUE, SUITE 128 PORT WASHINGTON, NY 11050			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/722,934

Applicant(s)

LANE ET AL.

Examiner

Alexander O. Williams

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 21-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 21-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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Serial Number: 10/722934 Attorney's Docket #: YOR920030505US1(163-21)
Filing Date: 11/26/03;

Applicant: Lane et al.

Examiner: Alexander Williams

Applicant's Amendment filed 4/18/05 to the election with traverse of Group I (device claims 1-9) filed 6/4/04 is acknowledged.

Claims 10-20 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

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were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3 to 5, 8 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Lopatin et al. (US. Patent Application Publication # 2005/0101130 A1).

1. Lopatin et al. (figures 1 to 16e) specifically figure 16e show a solid state device comprising: a first material **10 or 6 or 20**; a second material **6 or 10 or 20**; a barrier layer **12** formed between the first material and the second material to prevent a diffusion between the first material and the second material, the barrier layer includes a metal form of at least one of Ru and Re.

DOCUMENT-IDENTIFIER: US 20050101130 A1

TITLE: Method and tool of chemical doping CoW alloys with Re for increasing barrier properties of electroless capping layers for IC Cu interconnects

----- KWIC -----

Summary of Invention Paragraph - BSTX (12):

[0010] The invention generally provides a method for forming a capping layer exhibiting enhanced barrier resistance to both copper and oxygen diffusion for a metal interconnect in a semiconductor device comprising, forming a capping layer on a conductive surface of the metal interconnect, wherein the capping layer comprises cobalt (Co), tungsten (W), rhenium (Re), and at least one of phosphorus (P) and boron (B), and annealing the capping layer. In another embodiment, the capping layer may further comprise at least one of calcium (Ca), aluminum (Al), nickel (Ni), and molybdenum (Mo).

Summary of Invention Paragraph - BSTX (13):

[0011] In another embodiment, the invention generally provides a method for forming a multilayer capping layer exhibiting enhanced barrier resistance to both copper and oxygen diffusion for a metal interconnect in a semiconductor device comprising, forming multiple layers and annealing the layers to form an interface layer, such that the interface layer comprises Co, W, Re, and at least one of P and B. In another embodiment,

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the multilayer capping layer may further comprise at least one of Ca, Al, Ni, and Mo.

3. The device as recited in claim 1, Lopatin et al. show wherein the first material **10** is a dielectric and the second material **6** is a metal.

4. The device as recited in claim 1, Lopatin et al. show wherein the first material **6 or 20** is a conductor and the second material is a metal **6 or 20**.

5. The device as recited in claim 1, Lopatin et al. show wherein the first material **6** includes copper.

8. The device as recited in claim 1, Lopatin et al. show wherein device is a semiconductor device and the first material includes a semiconductor material .

22. Lopatin et al. (figures 1 to 16e) specifically figure 16e show a solid state device comprising: a first material **10 or 6 or 20**; a second material **6 or 10 or 20**; a barrier layer **12** formed between the first material and the second material to prevent a diffusion between the first material and the second material, the barrier layer includes a metal form of **Re**.

Claims 1, 5, 8 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by D'urso et al. (US. Patent Application Publication # 2005/0095855 A1).

1. D'urso et al. (figures 1 to 13) specifically figure 7 show a solid state device comprising: a first material **42 or 34**; a second material **42 or 34**; a barrier layer **40** formed between the first material and the second material to prevent a diffusion between the first material and the second material, the barrier layer includes a metal form of at least one of **Ru** and **Re**.

DOCUMENT-IDENTIFIER: US 20050095855 A1

TITLE: Compositions and methods for the electroless deposition of NiFe on a work piece

----- KWIC -----

Detail Description Paragraph - DETX (5):

[0016] Referring to FIG. 4, a first conductive barrier layer 40 then may be formed overlying work piece 30 and within trench 36. First conductive barrier layer 40 prevents or minimizes the diffusion of copper through dielectric layer 34 and permits or facilitates the deposition of copper overlying dielectric layer 34. First conductive barrier layer 40 may comprise one conductive layer or more than one conductive layer. First conductive barrier layer 40 may be formed of tantalum (Ta),

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tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tantalum silicon nitride (TaSiN), cobalt (Co), ruthenium (Ru), rhodium (Rh), palladium (Pd), or any other suitable metal that hinders or prevents copper from diffusing into or otherwise adversely reacting with surrounding materials. In a preferred embodiment of the present invention, first barrier layer 40 is formed of tantalum. First conductive barrier layer 40 may be deposited using physical vapor deposition (PVD), ionized metal plasma (IMP), chemical vapor deposition (CVD) or any other suitable technique known in the semiconductor industry.

3. The device as recited in claim 1, D'urso et al. show wherein the first material **34** is a dielectric and the second material **42** is a metal.

5. The device as recited in claim 1, D'urso et al. show wherein the first material **42** includes copper.

8. The device as recited in claim 1, D'urso et al. show wherein device is a semiconductor device and the first material includes a semiconductor material.

21. D'urso et al. (figures 1 to 13) specifically figure 7 show a solid state device comprising: a first material **42 or 34**; a second material **42 or 34**; a barrier layer **40** formed between the first material and the second material to prevent a diffusion between the first material and the second material, the barrier layer includes a metal form of **Ru**.

Initially, and with respect to claims 6 and 7, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 6, 7 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lopatin et al. (US. Patent Application Publication # 2005/0101130 A1).

9. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in

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a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claims 6 and 7, as to the grounds of rejection under section 103, see MPEP § 2113.

Claims 6, 7 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over D'urso et al. (US. Patent Application Publication # 2005/0095855 A1).

9. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claims 6 and 7, as to the grounds of rejection under section 103, see MPEP § 2113.

Claims 2 and 23 to 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lopatin et al. (US. Patent Application Publication # 2005/0101130 A1) in view of Matsuse et al. (U.S. Patent Application Publication # 2002/0197856 A1).

Lopatin et al. Is cited for showing the features of the claimed invention as detailed above, but fail to explicitly show wherein the metal form includes a hexagonal close packed structure and wherein the metal is copper.

Matsuse et al. Is cited for showing a barrier film wiring structure and electrodes of semiconductors device having a barrier film. Specifically, Matsuse et al. (figures 1 to 14) specifically figure 1 discloses A solid state device comprising: a first material **8 or 15 or 4**; a second material **16**; a barrier layer **14** formed between the first material and the second material to prevent a diffusion between the first material and the second material, the metal form includes a hexagonal close packed structure for the purpose of having a low amount of oxygen contamination and high thermal stability.

2. The device as recited in claim 1, the combination with Matsuse et al. show wherein the metal **16** form includes a hexagonal close packed structure (see **16** in figure 1).

23. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is

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said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one of ordinary skill in the art to use Matsuse et al.'s metal form including a hexagonal close packed structure to modify Lopatin et al.'s metal form for the purpose of having a low amount of oxygen contamination and high thermal stability.

Claims 2, 23, 24, 26 and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over D'urso et al. (US. Patent Application Publication # 2005/0095855 A1) in view of Matsuse et al. (U.S. Patent Application Publication # 2002/0197856 A1).

D'urso et al. Is cited for showing the features of the claimed invention as detailed above, but fail to explicitly show wherein the metal form includes a hexagonal close packed structure and wherein the metal is copper.

Matsuse et al. Is cited for showing a barrier film wiring structure and electrodes of semiconductors device having a barrier film. Specifically, Matsuse et al. (figures 1 to 14) specifically figure 1 discloses A solid state device comprising: a first material **8 or 15 or 4**; a second material **16**; a barrier layer **14** formed between the first material and the second material to prevent a diffusion between the first material and the second material, the metal form includes a hexagonal close packed structure for the purpose of having a low amount of oxygen contamination and high thermal stability.

2. The device as recited in claim 1, the combination with Matsuse et al. show wherein the metal **16** form includes a hexagonal close packed structure (see 16 in figure 1).

23. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one of ordinary skill in the art to use Matsuse et al.'s metal form including a hexagonal close packed structure to modify

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D'urso et al.'s metal form for the purpose of having a low amount of oxygen contamination and high thermal stability.

Response

Applicant's arguments filed 4/11/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

Field of Search	Date
U.S. Class and subclass: 257/751,758,773,774,759,760,762	8/18/04 2/7/05 6/14/05
Other Documentation: foreign patents and literature in 257/751,758,773,774,759,760,762	8/18/04 2/7/05 6/14/05
Electronic data base(s): U.S. Patents EAST	8/18/04 2/7/05 6/14/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30 AM -7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
6/15/05



Primary Patent Examiner
Alexander O. Williams